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SF-8336

B. E. III (Sem. VI) (EC/ECC) Examination

May / June – 2011

VLSI Technology & Design

(New Syllabus)

Time : **3** Hours] [Total Marks : **100**

Instructions :

(1)

નીચે દર્શાવેલ ☛ નિશાનીવાળી વિગતો ઉત્તરવહી પર અવશ્ય લખવી.
Fillup strictly the details of ☛ signs on your answer book.

Name of the Examination :

☛ **B. E. 3 (Sem. 6) (EC/ECC)**

Name of the Subject :

☛ **VLSI Technology & Design (New)**

☛ Subject Code No. : **8 3 3 6** ☛ Section No. (1, 2,.....) : **Nil**

Seat No. :

Student's Signature

(2) Attempt all questions.

(3) Assume suitable data wherever required.

(4) Figure to the right indicate full marks.

1 (a) Answer the following questions : **10**

(i) Draw Combined energy band diagram of MOS structure. **3**

(ii) Explain following terms : **3**

(a) Electron effinity

(b) work function

(c) Fermi Potential.

(iii) Explain Noise Margin. **2**

(iv) Draw the symbols of N channel and P channel MOSFET. **2**

(b) What do you mean by MOSFET Scaling ? Explain Constant-field Scaling and Constant-voltage Scaling in detail. **10**

2 (a) Describe Accumulation,. Depletion and Inversion process for the MOS system under eternal bias. Also derive the equation for maximum depletion region depth at the onset of surface inversion. **8**

(b) Explain CMOS ring Oscillator in detail. **8**

OR

2 (a) Explain CMOS inverter in detail. 8

(b) Derive the equation of Drain current for an N-channel MOSFET operating in all linear region. Draw the necessary sketch. 8

3 Attempt any **two** : 14

(i) Write short note on CMOS NOR2 Gate.

(ii) Explain short channel effect.

(iii) Explain SR latch circuit using sequential MOS logic circuit.

4 (a) Answer the following : 10

(i) Differentiate between full custom design and semi custom design.

(ii) Define terms : regularity and modularity.

(iii) Define terms : Lithography and photo resist.

(iv) Draw dynamic D-latch circuit.

(v) Define terms : controllability and observability.

(b) Draw domino CMOS circuit for Z=AB+(C+D)(E+F) + GH 6

(c) Compare FPGA with CPLD. 4

5 (a) Explain VLSI design flow with Gajski chart. 8

(b) Explain fabrication steps of NMOS Transistor with necessary diagram.

OR

5 (a) Prove that NMOS transistor transfer strong "0" Logic and weak "1" Logic. 8

(b) Draw and explain dynamic shift register with ratioed logic. 8

6 Attempt any **two** : 14

(a) Explain LOCOS with necessary diagrams.

(b) Explain FPGA with necessary diagram.

(c) Explain Latch-up and its prevention.

(d) Explain computer aided design technology in details.
